Investigation of Surface Potential for Double Gate Hetero Junction Tunnel FinFET:Application to high-*k* material HfO_2

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***Abstract*— Tunnel FETs (TFETs) shown to be the promising devices for low standby power applications but suffers from low ON and high threshold voltage. The hetero junction tunnel FinFET has been studied here to overcome these limitations. In this work, surface potential has been modeled for double gate hetero junction tunnel FinFET to optimize the performance. Surface potential derived by applying the solution of 2-D Poisson equation and it is developed using superposition technique.The high-*k* dielectric material HfO_2 on the surface potential model is also addressed.The analytical predictions are compared with the results obtained by the 2-D numerical techniques and Technology Computer Aided Design (TCAD) simulator (Synopsys TCAD), the obtained results are almost similar.**

Keywords— FinFET,TFET,TCAD, ITRS

I. INTRODUCTION

Since the invention of IC by J. Kilbey in 1958 [1] many advances took place in Electronics. Prior to this breakthrough the computation was expensive venture and computational equipment engaged a large space. Nowadays everybody is carrying a personal computer in their pockets. The back bone for this revolution is the man Gordon E. Moore's inspection of doubling the density of the transistors on the chip, which has been following for the last four decades to develop the performance and to decrease the cost such that cost per function reduces [2]. So that additional functions can be integrated at the similar cost. The delay gets reduced, there by the operating frequency increases and results increase in speed. As well with the scaling of the applied potential the power dissipation gets reduced [3]. In view of the fact that for the same functionality the die area is reduced by the square of the gate length so the defects per die is reduced.FinFET had chosen to continue the scaling at 22 nm and beyond by Intel in 2013 [4]. Scaling of the fin body thickness pushing the trigateFinFET to reach limits in the performance. For the technology nodes beyond 16/14 nm the gate dielectric stack thickness is less than 1 nm as for ITRS 2013 [5]. FinFET is developed with special emphasis on process simplicity and compatibility with conventional planar CMOS technology. Devices with gate length of 18 nm and gate oxide thickness of 2.5 nm have been experimentally demonstrated with acceptable short-channel characteristics. There are two main types of FinFETs: Bulk FinFET and SOI FinFET. A basic structure of bulk and silicon-on-insulator (SOI) FinFETs are shown in Fig.1. TFETs are the emerging devices with SS less than 60mV/dec shown to be the ultimate solution for the future low standby power applications [6]. Unlike conventional MOSFETs these devices conduct because of the band to band tunneling at the source/drain
junction. Differenttypes of the tunnel FET structures have been proposed in the literature for better performance [7]-[8].

Homojunction tunnel FETs made of Si are suffering from the low I_{ON} currents and high threshold voltage. To overcome these problems hetero junction TFETs have been studied [9]-[10]. As the gate oxide thickness shrinkages nearly 1 nm the gate tunnelling current (leakage current) increases significantly due to quantum tunneling effect [11]. This enormous gate leakage current will be a difficulty for decreasing gate oxide thickness for the future high speed electronic devices. Consequently as the channel length is reduced, the gate oxide thickness is essential to be reduced proportionally in order maintain different short channel effects (SCE's). Thinning the gate oxide greater the drive current, which gives the increase speed in integrated circuit's. But there is a boundary for SiO_2 as the gate dielectric material due to large tunnelling current owing to direct tunnelling. Therefore there is a prospect to employ high-*k* dielectric materials for gate dielectric as an alternative material for future CMOS technology [12]. Out of the different high-*k* dielectric materials, HfO_2 is one of the promising materials for this purpose [13]-[14].

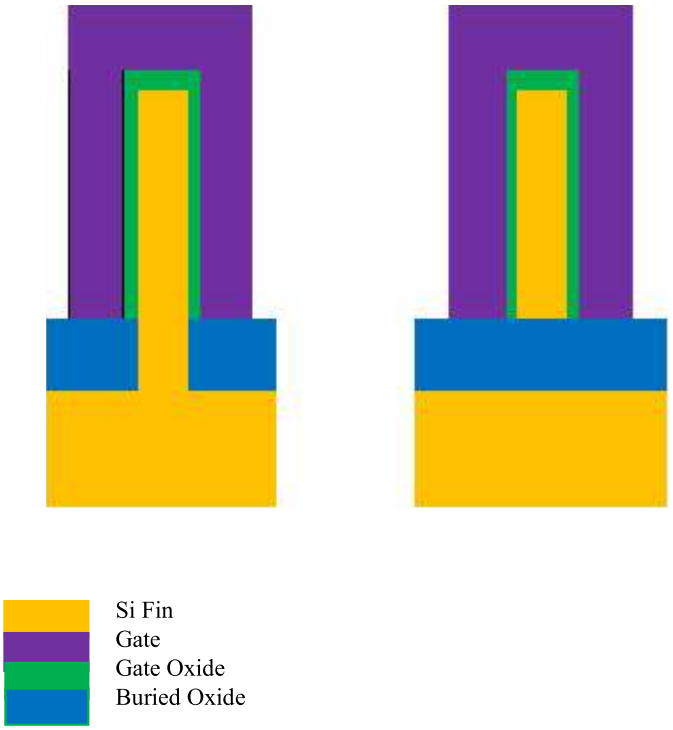

Fig.1. Basic structure of Bulk FinFETand SOI FinFET

In this work the hetero junction tunnel FinFET with source overlap is simulated and validated through mathematical modelling.Theoretical estimates are compared with the results acquired by the 2-D numerical device simulator Synopsys TCAD for standard SiO_2 material, excellent agreements between them are perceived. This paper also extends the model to include the selected high-*k* dielectric material HfO_2 for analysis.

The paper is organized as follows: Section II presents the Analytic modelling. Section III comprises result and Finally, section IV concludes the paper.

II. ANALYTICAL MODELLING

Figure 2 shows the 2-D cross section structure of the hetro junction tunnel FinFET. In view of the fact that the top gate oxide prepared thicker than the side gate oxide accordingly it can be approximated to the double gate operation. We know the 2-D poisson equation concerning the inversion carriers can be written as[15].

$$\frac{\partial^2\psi}{\partial x^2}+\frac{\partial^2\psi}{\partial y^2}=\left(\frac{q}{\varepsilon_{Si}}\right)n_i e^{\left(\frac{\psi-V}{\phi_t}\right)}$$

Here $\psi(x,y)$ is the electrostatic potential, ε_{Si} is the permittivity of the Si, n_i is the intrinsic carrier density, $\phi_t = kT/q$, and k is the Boltzman constant, and q is electronics charge. So, can be written as, $\psi(x,y)=v(x)+\psi_1(x,y)$.Where $v(x)$ is the solution of 1-D Poisson's equation $\left[\partial^2 v/\partial x^2\right]=\left[(q/\varepsilon_{Si})\,n_i e^{((\psi-V)/\phi_t)}\right]$.

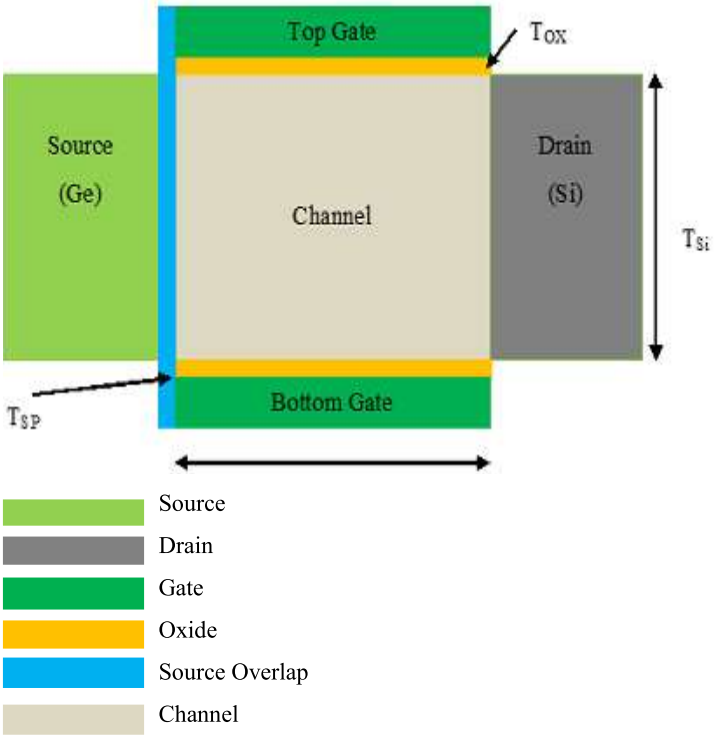

Fig.2. 2-D cross section of the hetero junction tunnel FinFET

After integrating twice and can be solved by applying the boundary conditions at the semiconductor-oxide interface,

$$\left[\left(\frac{(V_{GS}-\Delta\phi-V)}{2\phi_t}\right)+\ln\left\{\left(\frac{T_{Si}}{2}\right)\left(\sqrt{\frac{qn_i}{2\varepsilon_{si}\phi_t}}\right)\right\}\right]==\ln(\beta)-\ln(\cos\beta)-\left[\left(\frac{2\varepsilon_{si}T_{OX}}{\varepsilon_{ox}T_{si}}\right)\beta\tan\beta\right] \quad (2)$$

where φ is work function difference between the gate electrode and the semiconductor, $\beta=(T_{Si}/2)\left(\sqrt{C_1}/2\phi_t\right)$, C_1 is integrating constant and ε_{ox} is the permittivity of the insulator. Since the current flows mainly along the channel from the source to the drain, the electron quasi Fermi potential is almost constant in x-direction and varies only in y-direction. Similar to MOSFETs, TFETs simulations demonstrate that V in the channel length direction stays constant except at the beginning of the channel. $\psi_1=(x,y)$ is the solution to the 2-D Laplace equation $\left[\left(\partial^2\psi_1/\partial x^2\right)+\left(\partial^2\psi_1/\partial y^2\right)\right]=0$. Using superposition, the electrostatic potential in the double gate tunnel FinFET can be, $\psi_1(x,y)=u_L(x,y)+u_R(x,y)$. If we are assuming the source terminal and drain terminal junctions are abrupt, using boundary conditions the solution can be written as,

$$\left[\psi_1(x,y)\right]=\left[C_1\sin(\lambda_n x)\sinh(\lambda_n y)\right]+\left[C_2\sin(\lambda_n x)\cosh(\lambda_n y)\right] \quad (3)$$

According to Superposition theorem,

$$u_L=C_2\sin(\lambda_n x)\sinh(\lambda_n y)$$

and

$$u_R=C_3\sin(\lambda_n x)\sinh(\lambda_n y)$$

By applying the boundary conditions,

$$u_L=\left\{\begin{array}{l} C_2\sin\left(\lambda_n\left(x+T_{Si}/2\right)\right)\sinh(\lambda_n(L-y)) \\ C_2\sin\left(\lambda_n\left(x+T_{OX}+\frac{T_{si}}{2}\right)\right)\sinh(\lambda_n(L-y)) \\ C_2\sin\left(\lambda_n\left(x-T_{OX}-\frac{T_{si}}{2}\right)\right)\sinh(\lambda_n(L-y)) \end{array}\right\} \quad (4)$$

According to Fourier series we can write for $-\frac{T_{Si}}{2} < x < \frac{T_{Si}}{2}$: for body,

$$\left[\frac{E_G}{2q}\right] = \sum_{n=1}^{\infty} \mathrm{C_n} \left\{ \sin\left(\lambda_n \left(x + \frac{T_{Si}}{2} \right) \right) \right\} \tag{5}$$

Similarly $-T_{OX} - \frac{T_{Si}}{2} < x < -\frac{T_{Si}}{2}$: for top gate,

$$\left[\frac{E_G}{2q}\right] = \sum_{n=1}^{\infty} \mathrm{C_{Tn}} \left\{ \sin\left(\lambda_n \left(x + T_{OX} + \frac{T_{Si}}{2} \right) \right) \right\} \tag{6}$$

and $\frac{T_{Si}}{2} < x < T_{OX} + \frac{T_{Si}}{2}$: for bottom gate,

$$\left[\frac{E_G}{2q}\right] = \sum_{n=1}^{\infty} \mathrm{C_{Bn}} \left\{ \sin\left(\lambda_n \left(x - T_{OX} - \frac{T_{Si}}{2} \right) \right) \right\} \tag{7}$$

Here $\sum_{n=1}^{\infty} \mathrm{C_n} = \mathrm{C_2} \sinh\left(\lambda_n L\right)$, $\sum_{n=1}^{\infty} \mathrm{C_{Tn}} = \mathrm{C_2} \sinh\left(\lambda_n L\right)$,

and $\sum_{n=1}^{\infty} \mathrm{C_{Bn}} = \mathrm{C_2} \sinh\left(\lambda_n L\right)$,

at this moment the equations will be,

$$U_L(x,y) = \left\{ \begin{array}{l} \sum_{n=1}^{\infty} \frac{C_n}{\sinh(\lambda_n L)} \sin(\lambda_n (x + A)) \sinh(\lambda_n (L - y)) \\ \sum_{n=1}^{\infty} \frac{C_{Tn}}{\sinh(\lambda_n L)} \sin\left(\lambda_n \left(x + T_{OX} + \frac{T_{Si}}{2} \right) \right) \sinh(\lambda_n (L - y)) \\ \sum_{n=1}^{\infty} \frac{C_{Bn}}{\sinh(\lambda_n L)} \sin\left(\lambda_n \left(x - T_{OX} - \frac{T_{Si}}{2} \right) \right) \sinh(\lambda_n (L - y)) \end{array} \right\}$$

and

$$U_R(x,y) = \left\{ \begin{array}{l} \sum_{n=1}^{\infty} \frac{B_n}{\sinh(\lambda_n L)} \sin(\lambda_n (x + A)) \sinh(\lambda_n (y)) \\ \sum_{n=1}^{\infty} \frac{B_{Tn}}{\sinh(\lambda_n L)} \sin\left(\lambda_n \left(x + T_{OX} + \frac{T_{Si}}{2} \right) \right) \sinh(\lambda_n (y)) \\ \sum_{n=1}^{\infty} \frac{B_{Bn}}{\sinh(\lambda_n L)} \sin\left(\lambda_n \left(x - T_{OX} - \frac{T_{Si}}{2} \right) \right) \sinh(\lambda_n (y)) \end{array} \right\}$$

. (9)

Using dielectric boundary conditions at bothsemiconductor-oxideinterfaces and taking ratios of these results yields an Eigen value equation for the scale length,

$$\varepsilon_{Si} \tan\left(\frac{\pi T_{OX}}{\lambda_n} \right) = \varepsilon_{OX} \tan\left(\pi \left(A - \frac{T_{Si}}{2} \right) / \lambda_n \right) =$$

$$-\varepsilon_{OX} \tan\left(\pi \left(A + \frac{T_{Si}}{2} \right) / \lambda_n \right) \tag{10}$$

The Eigen value equation for the scale length then turn into, $\varepsilon_{Si} \tan\left(\left(\pi T_{OX} \right) / \lambda_n \right) = \varepsilon_{OX} \tan\left(\left(n\pi / 2 \right) - \left(\pi T_{Si} / 2\lambda_n \right) \right)$. This equation is found that $\lambda_1 > \lambda_2 > \lambda_3 ..... \lambda_n$ also $\left(\frac{\lambda_n}{\lambda_1} \right) \approx \left(\frac{1}{n} \right)$. Now u_L and u_R can be written as,

$$u_R = \sum_{n=1}^{\infty} \mathrm{B_n} u_{Rn}(x,y); u_L = \sum_{n=1}^{\infty} \mathrm{C_n} u_{Ln}(x,y)$$

Where

$$u_{Ln}(x,y) = \left\{ \begin{array}{l} \sum_{n=1}^{\infty} \frac{\sinh \frac{\pi (L - y)}{\lambda_n}}{\sin\left(\frac{\pi T_{OX}}{\lambda_n} \right)} \frac{\sinh(\lambda_n (L - y))}{\sinh(\lambda_n L)} \sin\left(\frac{n\pi}{2} + \frac{\pi x}{\lambda_n} \right) \\ \sum_{n=1}^{\infty} \frac{\sin\left(\frac{n\pi}{2} - \frac{T_{Si}}{2\lambda_n} \right)}{\sin\left(\frac{\pi T_{OX}}{\lambda_n} \right)} \frac{\sinh(\lambda_n (L - y))}{\sinh(\lambda_n L)} \sin \lambda_n \left(x + T_{OX} + \frac{T_{Si}}{2_n} \right) \\ \sum_{n=1}^{\infty} \frac{\sin\left(\frac{n\pi}{2} + \frac{T_{Si}}{2\lambda_n} \right)}{\sin\left(\frac{\pi T_{OX}}{\lambda_n} \right)} \frac{\sinh(\lambda_n (L - y))}{\sinh(\lambda_n L)} \sin \lambda_n \left(x - T_{OX} - \frac{T_{Si}}{2_n} \right) \end{array} \right\}$$

$$u_{Rn}(x,y)=\begin{cases}\displaystyle\sum_{n=1}^{\infty}\frac{\sinh\frac{\pi y}{\lambda_n}}{\sin\left(\frac{\pi T_{OX}}{\lambda_n}\right)}\frac{\sinh(\lambda_n(y))}{\sinh(\lambda_n L)}\sin\left(\frac{n\pi}{2}+\frac{\pi x}{\lambda_n}\right)\\ \displaystyle\sum_{n=1}^{\infty}\frac{\sin\left(\frac{n\pi}{2}-\frac{T_{Si}}{2\lambda_n}\right)}{\sin\left(\frac{\pi T_{OX}}{\lambda_n}\right)}\frac{\sinh(\lambda_n(y))}{\sinh(\lambda_n L)}\sin\lambda_n\left(x+T_{OX}+\frac{T_{Si}}{2_n}\right)\\ \displaystyle\sum_{n=1}^{\infty}\frac{-\sin\left(\frac{n\pi}{2}+\frac{T_{Si}}{2\lambda_n}\right)}{\sin\left(\frac{\pi T_{OX}}{\lambda_n}\right)}\frac{\sinh(\lambda_n(y))}{\sinh(\lambda_n L)}\sin\lambda_n\left(x-T_{OX}-\frac{T_{Si}}{2_n}\right)\end{cases}$$

The Eigen functions are not orthogonal that is the integral $\int_{-\frac{T_{Si}}{2}-T_{OX}}^{\frac{T_{Si}}{2}+T_{OX}} u_{Ln}(x,0)u_{Lm}(x,0)dx$ for $(n\neq m)$ not necessarily zero.After neglecting the conditionsapart from the largest Eigen value term,for symmetric double gate the series decay even faster because the even coefficients are zero. So,

$$\psi(x,y)=v(x)+\cos\left(\frac{\pi x}{\lambda_1}\right)\left(\frac{b_1\sinh\left(\frac{\pi(L-y)}{\lambda_1}\right)+c_1\sinh\left(\frac{\pi y}{\lambda_1}\right)}{\sinh\left(\frac{\pi L}{\lambda_1}\right)}\right)$$

The above equation is used to match the surface potential in the channel. The corresponding of the surface potential with TCAD is able by making an allowance for the parameters of the Ge for $y=0$ to $y=T_{SP}$ designed for the overlapped region and parameters of the Si from $y=T_{SP}$ to $y=T_{SP}+L$.

III. RESULTS AND DISCUSSION

The surface potential analytical model for the tunnel FinFET is devised by solving the 2-D Poisson equation in the channel region. It is also considered for overlap region. In this model, the channel region charge is well thought-out. So the investigative model is applicable for the all the regions of operation for the selected device. The structure consisting of high-k dielectric material HfO_2, is used to verify the surface potential model against the 2-D device simulator, a commercial TCAD of Synopsys for a wide variation of distance along the channel (0 to 200 nm) having length is 50 nm. The gate to source voltage is varies 0 and 0.6 V. The drain to source voltage is fixed at 0.7 V. The examination for the surface potential is limited to room temperature. Hence any change in the current flow can be neglected due to thermal involvement. For device simulation, a self-consistent surface potential model has been used, that aids in the study of deep sub micronFinFET, therefore correctly calculate the surface potential. The surface potential of the double gate tunnel FinFET with source overlap both TCAD simulation and the analytical model is shown in Fig. 3.It shows the model is in good agreement with the simulated result.

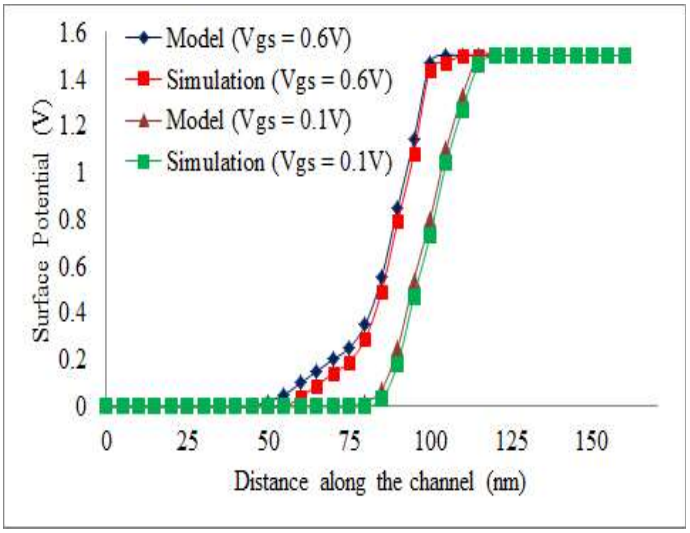

Fig. 3.Surface potential of simulated and model values for double gate tunnel FinFET on behalf of SiO_2 material

The surface potential and distance along the channel characteristics with the effective oxide thickness (EOT) of 1.35 nm as a parameter for the HfO_2 is depicted in Fig. 4. This figure clearly shows that using high-k material the surface potential is increasing, due to the fringing field lines from the bottom of the gate electrode. As a result, the charges are induced in the drain and source regions. It also shows that the model is in good agreement with the TCAD simulated result. Fig. 5 shows the drain current and gate voltage characteristics (I_D-V_G characteristics) for the device with different effective oxide thickness are 1.35 nm, 1.5 nm and 2.35 nm) having length is 50 nm. Here also the drain to source voltage is fixed at 0.7 V.

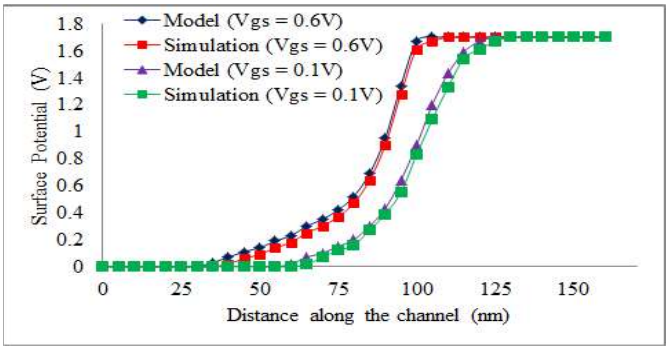

Fig. 4. Surface potential of simulated and model values for double gate tunnel FinFET on behalf of HfO_2 material

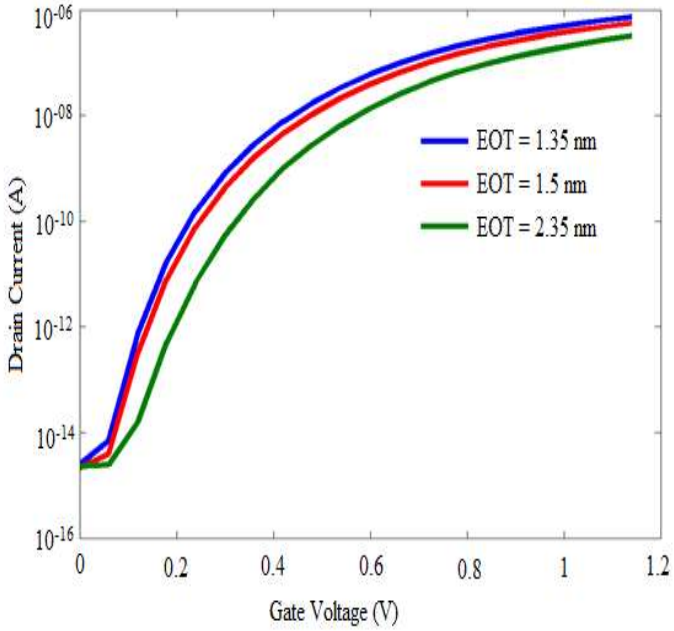

Fig. 5. I_D-V_G Characteristics of tunnel FinFET for different EOT

IV. Conclusion

This paper has suggested a surface potential model for double gate heterojunction FinFETconsisting of SiO_2 along with high-*k* dielectric material, HfO_2. A comparison has been made with accurate two dimensional device simulations. From the proposed analytical model, it is clear that the calculated values of the surface potential obtained, agree fine with the TCAD simulated results. Due to the fringing field effects from the bottom of the gate electrode the surface potential value has increased for high-*k* dielectric material, HfO_2.

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